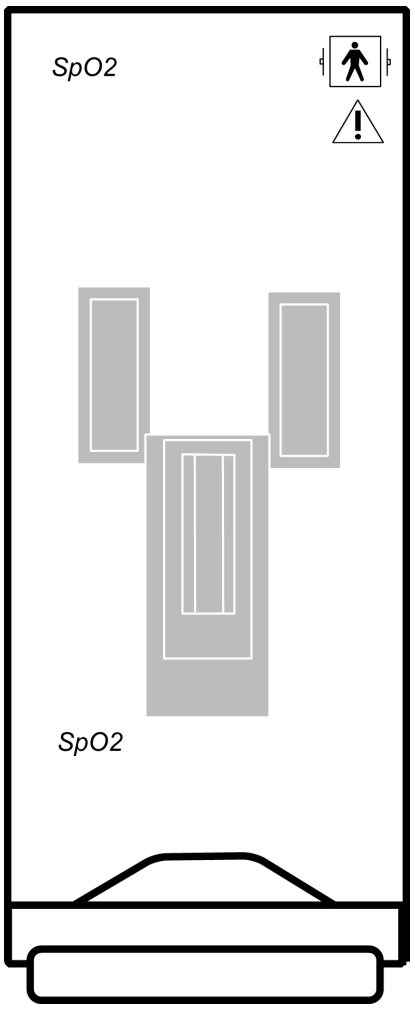
SPO2 MODULE

INTRODUCTION

This area contains service information about the Model 7310 Pulse Oximetry Module. The SpO2 Module monitors functional oxygen saturation of arterial blood by calculating the ratio of oxygenated hemoglobin to hemoglobin that is capable of transporting oxygen. It provides continuous, noninvasive measurements of SpO2 and can display a plethysmographic waveform. Heart rate values are also derived from the pulse oximetry signal.



PHYSICAL DESCRIPTION

The SpO2 module, shown in FO-32B, is enclosed in a single wide module enclosure. The module consists of two rigid PWAs, a front sensor flex connector, interconnect cabling, and the mechanical enclosure components. The digital PWA, with its PNet interface connector, occupies the left slot in the module enclosure (when viewed from the sensor connector end of the module), and the OEM PWA, with shield/mounting assembly, occupies the right slot in the module enclosure.

FUNCTIONAL PRINCIPLES OF OPERATION

A functional block diagram of the SpO2 Module is shown in FO-32A. The diagram is divided into isolated circuitry and non-isolated circuitry. The isolated circuitry includes the SpO2 sensor, the flex PWA, and the OEM PWA. The isolated (ISO) interface and DC-DC converter isolate this circuitry from the non-isolated core logic.

The core logic provides communication between the system host and Module through the PNet synchronous serial interface. It also includes an asynchronous data channel to the OEM PWA and controls the isolated DC-to-DC convertor.

Isolated Circuits

Isolated circuits are shown in the top half of FO-32A. Signals from the SpO2 sensor are conditioned, digitized, and processed on the OEM PWA. The SpO2 sensor is connected to the OEM PWA through a 9-pin D connector on the module front panel and flex PWA 313-112.

The isolated interface provides an opto-coupled asynchronous serial communication channel between the core logic and the OEM PWA.

The isolated power block consists of a monolithic DC-DC converter that provides +15V, +5V, and -15V to the OEM PWA.

Non-Isolated Circuits

Non-isolated circuits are shown in the bottom half of FO-32A. Functional blocks include the PNet interface, isolated power control, reset/failsafe, 68302 CPU, 128Kx8 data memory, 128Kx8 program memory, the model and serial number EEPROM, and logic analyzer/test interface.

Power (+12V and +5V), is received through J1. The +12V is applied to DC-to-DC converter PM100, which powers the isolated circuitry. ISO power control

controls PM100 power-on after the CPU is reset and shuts down PM100 if a failsafe condition occurs.

The Module will not be damaged when plugged into a live slot. Core logic power inputs to a Module are limited to a peak inrush current during hot-plugging. Within 2 seconds the Module responds to identification and wakes up in a minimized power state until registered with the system.

The PNet interface allows asynchronous and synchronous data transfer between the core logic and the external devices. Synchronous operation is always used in MPS systems. Asynchronous operation is for test and development only. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafe if a problem occurs with the microprocessor. The microprocessor controls and transfers data within the core logic. The program memory is a FLASH device that can be loaded with program information from the PNET interface or the logic analyzer interface. Data memory temporarily stores status and monitoring data for processing.

COMPONENT PRINCIPLES OF OPERATION

Schematic diagram of the SpO2 Digital PWA. The first sheet of the schematic shows an overall block diagram of the SpO2 digital PWA.

SpO2 Front End

EMI filtering at the front end is provided on the flex circuit and the OEM PWA. The PWA is also shielded. Signals are sent and received through front end connector J102 with the following pin-out:

PIN	NAME	PIN	NAME
1	RCAL	6	GND
2	+LED	7	SGND
3	-LED	8	Not Used
4	Not Used	9	CATHODE
5	ANODE		

The transducer plug shield is connected to shield ground (SGND).

OEM PWA

The OEM PWA supplies power to light the sensor LED. A waveform generated by the sensor photo-diode is applied to the PWA where it is conditioned, digitized, processed and sent to the isolated interface shown on sheet 7 of the schematic.

Isolated Power

The isolated power section provides patient isolation from earth ground by isolating the power for the patient connected circuitry. The isolated power supply is shown on sheet 7 of the schematic.

Power (+12V) is applied to DC-to-DC converter PM100 at +VIN and returned at -VIN. After the CPU is reset, ISO_PS-0 goes LOW and turns off Q102. This turns on Q100 and applies power to PM100. For reduced power operation when the Module is not in use, the program allows ISO_PS-0 to float, turning off the isolated power supply.

If a failsafe condition occurs, FS-1 will go HI, turn on Q103, turn off Q100, and shut down power to PM100. It will remain in the state until the failsafe is cleared.

PM100 provides isolated, regulated power outputs of ±15VDC (ISO_+15V and ISO_-15V) and +5V (ISO_+5V) to the OEM PWA. Q101 turns on the +5V supply after the +15V supply is up.

Isolated Interface

As shown on sheet 7 of the schematic, opto-couplers U100 and U101 provide a full duplex, isolated serial channel between the non-isolated core logic and the isolated circuitry. Q105 and Q106 buffer the signal to the opto-couplers.

Core Logic

The core logic is shown on sheets 2 through 7 of the schematic. The core logic provides communication between the system host and Module through the PNet synchronous serial interface. It also controls data acquisition and data processing functions for the SpO2 sensor. The Module is an 8-bit version of the core logic with one 128Kx8 RAM and 128Kx8 ROM device. The microprocessor runs at 9.416 MHz.

PNet Interface

The PNet interface, shown on sheet 2 of the schematic, provides the following functions:

- RS485 drivers (U7 and U8) for serial data and clock,
- Module select and presence detection (U2),
- Module synchronization.

Core signals are received on PNet connector J1 (sheet 2) with the following pin-out:

PIN	NAME	PIN	NAME
1A,1B	+5V	6B	M_SELECT
2A	DATA+	7A	M_PRESENT
2B	DATA-	7B	TXOC-0
3A,3B	+3.3V	8A	M_SYNC-0
4A	CLK+	8B	-12V
4B	CLK-	10A,10B	+12V
5A,5B	GROUND	1,2	GROUND
6A	M_RESET		

The SpO2 Module is designed to be hot-plugged, or inserted and removed from powered systems. Ground pins 1 and 2 are longer than the other connector pins, thus they make first and break last to protect circuitry. This is partially because of protective impedance located on the system backplane, in series with the Modules +5V and +12V power. Also series impedance on PNet control lines limits inrush and protects logic devices from excessive currents during a hot-plug power up.

The PNet protocol defines two modes of operation: synchronous and asynchronous. The normal mode of operation is synchronous, with half duplex transmitted and received data on differential signals DATA+ and DATA-. As shown on sheet 2 of the schematic, the device transmitting the serial data also generates differential clock signals CLK+ and CLK-. Transceiver direction for data and clock are controlled by the 68302 processor-generated TX_EN-0 (low true transmit enable) signal through U2. In the synchronous mode, both data and clock transceivers U7 and U8 are set to receive (i.e., transmit disabled) when fail-safe signal FS-0 is asserted.

The alternate serial mode, full duplex asynchronous, is entered by asserting processor generated control bit ASYCH_EN. This mode transmits data onto the differential signals CLK+ and CLK-, and receives data from the differential signals DATA+ and DATA-. The transmitter in the Module is disabled unless the Module has been commanded to transmit per the PNet protocol. The Module transmitter is immediately disabled after the last character of a transmission has been sent.

The Module select input (M_SELECT, hi true) instructs the Module to respond to identification requests. When both M_SELECT input and M_RESET input (hi true) are asserted, a Module performs a hardware reset.

The Module present output, M_PRESENT is connected to M_SELECT through diode CR1 to allow a means of determining if the Module is plugged into an instrument. When M_SELECT is asserted (pulled hi) M_PRESENT is hi true.

Module transmitter open collector signal TXOC-0 from Q1 signifies the Module transmitter is enabled. Serial data is then transmitted in the synchronous mode.

M_SYNC is used for timing of shorter latency periods than supported by the serial data protocols. A Module only asserts M_SYNC when enabled by the host.

Reset Logic

The reset logic is shown on sheet 3 of the schematic. Reset logic U9 generates a power-on-reset when power is applied. RESET-0 AND HALT-0 signals remain low for minimum of 130 msec after all logic voltages are in specification.

External reset, processor reset, and halt signals are low for minimum of 24 clocks when external reset asserted. Power monitoring, processor reset, and halt signals low if logic voltages drop below specification. They remain low for minimum of 130 msec after logic voltages return to the specified range.

The reset circuit (U6-4,5,6; U6-11,12,13) provides open drain outputs to the processor bi-directional reset and halt signals.

Fail-Safe Logic

Fail-safe latch (U6-1,2,3; U6-8,9,10) ensures that the Module enters a safe state if the processor fails to operate correctly. The latch is set by a low true output from the processor watchdog timer (WDOG-0). The data transmitter is disabled, isolated power is shut down, and the Module remains in a safe state until the latch is cleared by a power on or external reset.

Microprocessor

The core logic design is based around the 68302 microprocessor (U10) shown on sheet 4 of the schematic. The 68302 combines a 68000 core with a three channel communication processor, and system integration circuits.

The left side of the CPU contains clock interfaces to/from the PNet, port A, and port B to various circuits in the core logic, reset, and halt interface. The IRQ ports are not used. The right side of the CPU contains address and data lines and chip select outputs. The 68302 operates with a statically defined 8-bit wide bus. The following resources are used for specific Module functions:

CHIP SELECTS LOGIC

CS0-0	FLASH ROM
CS1-0	STATIC RAM

SERIAL COMM CHANNELS

SCC1	PNET [RXD1, TXD1, RCLK1, TCLK1, CTS1-0, RTS1-0]
SCC2	ASYNC DEBUG [RXD2,TXD2]
SCP	SERIAL EEPROM [SPRXD,SPTXD,SPCLK]
TIMER1	SYSTEM TIMEBASE

PARALLEL IO / SPECIAL PURPOSE IO BITS

PA2	CHIP SELECT TO SERIAL EEPROM
PA5	ASYCN_EN (PNET MODE SELECT)
PA6	POWER MANAGEMENT CONTROL
PB5 /TIN2	TIMEBASE INPUT FOR EXTERNAL MEMORY / SYSTEM CONFIG
PB7	WATCHDOG TIMER OUTPUT

Program Memory

Program memory consists of 8-bit flash ROM U11 shown on sheet 5 of the schematic. The ROM is configured for 128Kx8 (1024k bit). The ROM is not socketed and can not be removed for programming. The ROM can be flash-programmed via the logic analyzer interface or the PNET connector.

Data Memory

Data is stored in 128Kx8 static RAM U3. This RAM is cleared when power is removed.

Non-Volatile Memory

Serial EEPROM U1 is a 128-byte PROM that provides non-volatile storage for model and serial number information and parameter user interface data which must travel with the Module. The 68302 synchronous communication port (SCP) is used to access the EEPROM.

Logic Analyzer/Test Interface

The logic analyzer/test interface is shown on sheet 6 of the schematic. The core logic includes an interface to bring signals required for external ROM access, logic analyzer interface, and a debug serial channel to a single connector.

The external ROM access allows an off board ROM (8 bit) or ROMs (16 bit) to replace the FLASH devices at address 0. Address, data, and control signals required for this function are included on the LA/T connector.

All signals needed for a Hewlett Packard model 16500 logic analyzer or equivalent to perform bus state analysis and disassembly are included on the LA/T connector.

The 68302 SCC2 serial transmit and receive data signals are included on the LA/T connector.

The LA/T connector pinouts are as follows:

PIN	NAME	PIN	NAME
1,69	+5V	2,28,45,46,70	GND
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
29	D0	30	D1
31	D2	32	D3
33	D4	34	D5
35	D6	36	D7
37	D8	38	D9
39	D10	40	D11
41	D12	42	D13
43	D14	44	D15
47	DTACK-0	48	AS-0
49	RW	50	UDS-0
51	DS-0	52	BGACK-0
53	FC0	54	FC1
55	FC2	56	DEBUG TXD
57	DEBUGRXD	58	EXROMCS-0
63	PRGM_EN	64	DISCPU
65	T1_IN		

DISASSEMBLY PROCEDURE

STATIC DISCHARGE CAUTION

Do not attempt to service unit without static discharge protection. Workstations and personnel must be properly grounded, or damage to equipment will result.

1. Remove two 4-40 x 5-1/4" screws from the rear of the Module. Remove rear cover.

2. Carefully slide the enclosure away from the front panel, keeping the PWAs and front panel together.

3. Unsnap two tabs at top and two tabs at bottom of assembly, and remove insulators and card guides.

4. Carefully disconnect the cable from the digital PWA.

5. Remove the 4-40 x 1/4 screw (29, FO-32B) that fastens the flex circuit to the ground shield.

6. Disconnect the flex circuit from the PWA and remove the front cover/flex assembly.

7. Disassemble OEM shield assembly by disengaging each of the corner locking tabs (accessible through plastic shield vent openings).

8. Using FO-32B as a guide, perform any additional disassembly that may be required for maintenance procedures.

REASSEMBLY PROCEDURE

1. Make sure the fastening tabs on emi shield cover (23, FO-32B) for OEM PWA have not been deformed. Reassemble OEM PWA and shield assembly.

2. Carefully insert the front cover flex circuit into the connector on the PWA and secure with 4-40 screw (29).

3. Install digital PWA and connect 14-pin IDC interface connector.

4. Position flex circuit between PWA and sheild assembly and hold in place.

5. Push upper and lower card guides onto slots of assembly, and install insulators.

6. With enclosure oriented so large groove is at bottom and label is at right (viewed from front of Module), slide enclosure over front cover and attached PWA assembly.

7. Install back cover on the Module enclosure.

8. Fasten the front and rear covers to the enclosure by inserting two 4-40 x 5-1/4" screws from the rear through the enclosure to the front cover as shown in FO-32B. Tighten the two screws to 4-in/lb.

PARTS LISTS

Top Assembly 7310 parts are listed in Table 32-1 and shown in FO-32B. SpO2 Digital PWA 315-440 parts are listed in Table 32-2 and shown in FO-32C.

Table 32-1. Top Assembly 7310 Parts List

Item	Description	Part No.
1	COVER, PARAMETER REAR	703-188
2	SUB-ASSY, ENCLOSURE, EXTRUDED SW	320-676
3	C/A, SP02 NELLCOR, HOST	316-536
5	PANEL, FRONT SP02, NELLCOR	701-429
6	PWA, SP02, DIGITAL, NELLCOR	315-440
8	PWA, SP02 OEM, NELLCOR	*
10	INSULATION, GUIDE, MODULE	750-182
13	BUTTON, LATCH, SW	732-166
14	SPRING, CONTACT, GROUND	736-204
16	SCREW, 2-56X3/16 PNH PHH SST	719-237
17	SCREW, RDH PHH, 4-40X51/8, CUSTOM	722-201
18	INSULATOR, DIGITAL	750-189
19	SCREW, 4-40X1/4 PNH PHH SST	719-102
20	LATCH,CABLE RETENTION	759-328
22	PWA, FLEX, SP02 FRONT PANEL	313-112
23	EMI SHIELD COVER, SP02 NELLCOR	737-181
24	GASKET, WATER INGRESS SP02 NELLCOR	752-263
27	INSULATOR, NELLCOR PWA	750-188
29	SCREW, 4-40X1/4 PNH, PHH, SST	722-207
30	WASHER, FLAT #2 SST	723-402
31	EMI SHIELD ASSY, SP02	320-672

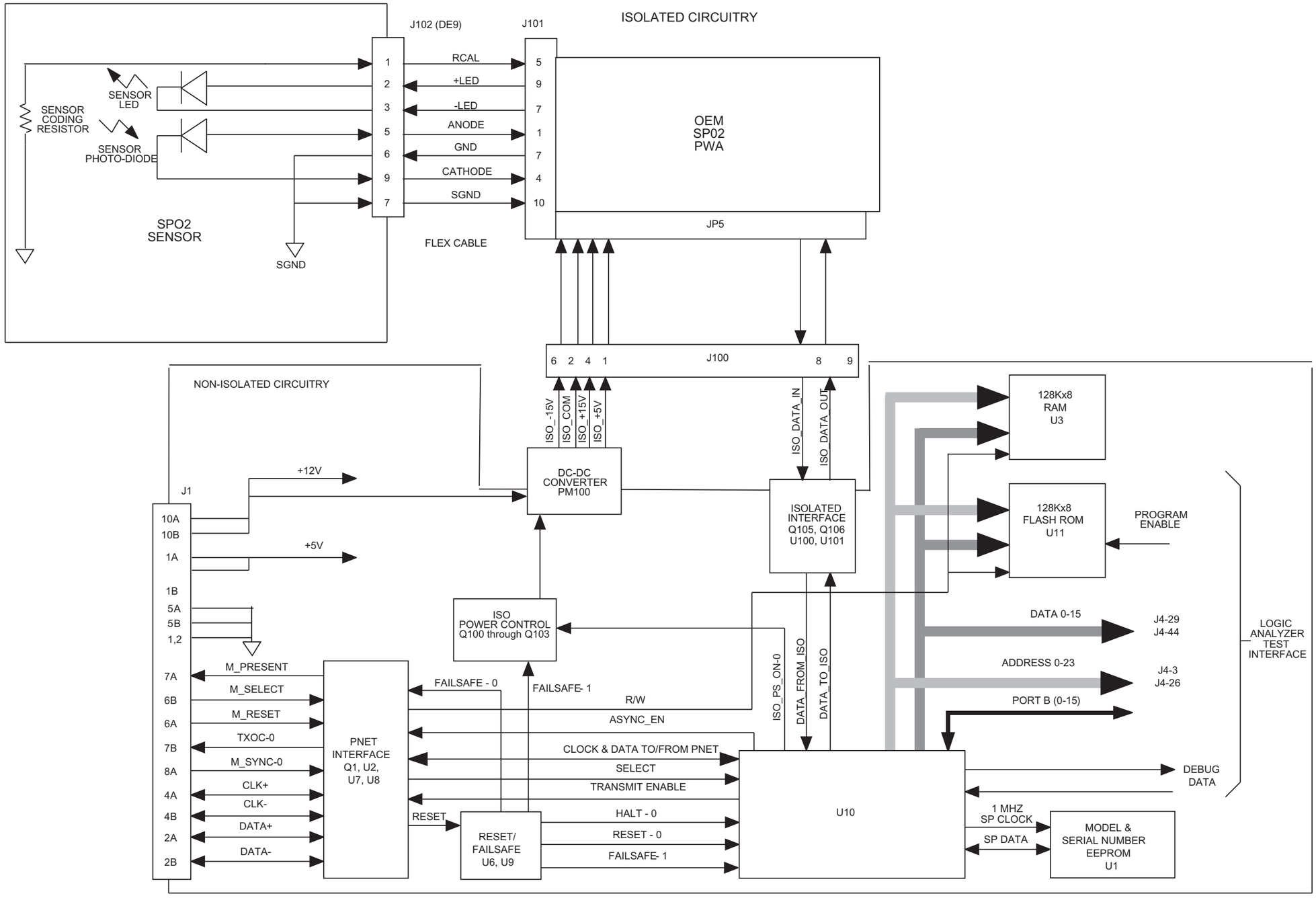
*This PWA cannot be ordered separately. If this PWA is defective, order replacement for the entire SpO2 Module.

Table 32-2. SpO2 Digital PWA 315-440 Parts List

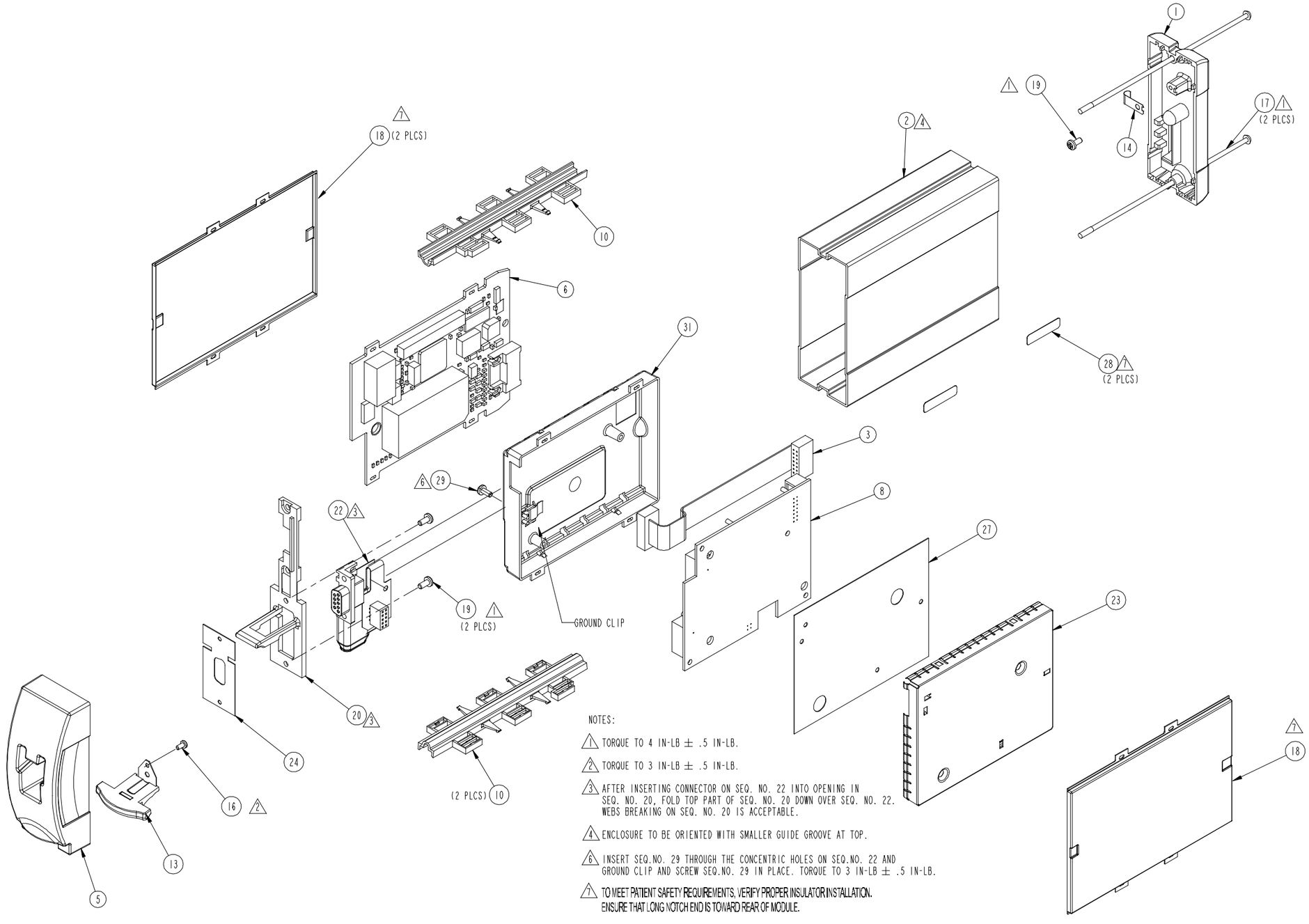
Item	Description	Part No.
C1,41	CAP,2917/D,TANT,35V,20%,10 UF	606-188
C2, 3	CAP,CER,SMD,0805,NPO,10%,50V,27 PF	605-418
C4-14, 16, 100-102	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
CR1,13	DIODE, SCHOTTKY, 30V, 200MW, SOT-23	611-137
CR2-7, CR10,11	DIODE, DUAL SERIES SMT SOT-23	611-140
CR12	DIO ZENER 6.2V, 5% SMT, 225MW	612-147
FB1-9	FERRITE CHIP, EMI SUPPRESSION, SMT	669-170
J1	CONN, 20 PIN PLUG RT ANGLE PC MOUNT	607-795
J4	SOCKET, MICRO STRIP 35X2, SMD	607-816
J100	HEADER, 14 PIN MALE RT. ANGLE .1 X .1	607-629 or 607-909
PM100	CONVERTER,DC/DC,THREE OUTPUT,+5,+15,-15	633-148
Q1	XST NPN 2222A SMT	674-127
Q100,101	XSTR, N-CHANNEL PWR MOSFET, DPAK	676-163
Q102,103	XSTR, N-CHAN MOS SOT-23	676-130
Q105,106	XST PNP SMT	674-126
R1,40,41,44 50,100,102, 104,111	RES,SMD,1/10W,1%,1.00K OHM	685-293
R2	RES,SMD,1/10W,1%,4.99K OHM	685-360
R3,4,7-33,35, 42,43,46-48, 101,103	RES,SMD,1/10W,1%,10.0K OHM	685-389
R5,6,105, 107,108	RES,SMD,1/10W,1%,2.21K OHM	685-326
R34	RES,SMD,1/10W,1%,698K OHM	685-566
R45	RES,SMD,1/10W,1%,100 OHM	685-197
R106, 109	RES,SMD,1/10W,1%,750 OHM	685-281

Table 32-2. SpO2 Digital PWA 315-440 Parts List (Continued)

Item	Description	Part No.
U1	IC,93C56 2KBIT SERIAL EEPROM,CMOS SM	692-183
U2	IC, EECMOS PLD 16V8B, ARRAY LOGIC	692-226
U4	IC,74AC32 QUAD 2 IN OR GATE,ADV CMOS SM	692-141
U6	IC,74HC03 QUAD 2 IN.NAND,CMOS SUF MT	692-139
U7,8	IC, CMOS LTC1485, DIFF BUS XCEIVER SO8	692-225
U9	IC, POWER SUPPLY MONT WITH RESET SMT	694-118
U10	IC, 68302 INTEGRATED PROCESSOR 144 SMT	694-130
U11	IC, 128K X 8-BIT 5V FLASH ROM CMOS SMT	692-195
U33	IC, 128X8 70NS CMOS SRAM TSOP	694-133
U100, 101	IC, HCPL-2611, OPTOCOUPLERS, SMT	695-101
Y100	CRYSTAL, 9.416MHZ, 0.005% HC-49UP	609-130
#39	PAL_U2A, CORE LOGIC	637-101



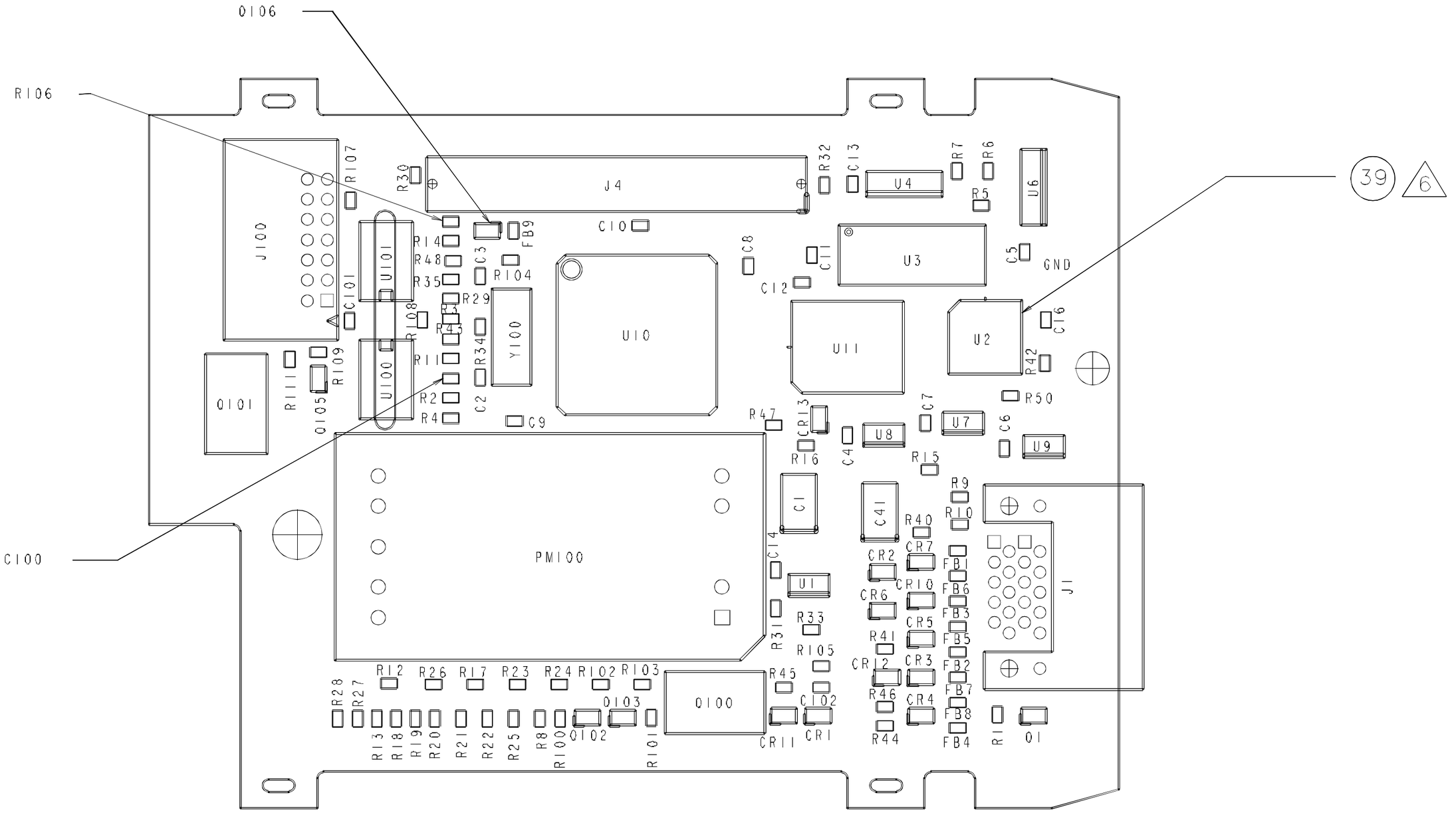
FO-32A. SpO2 Module Block Diagram



NOTES:

1. TORQUE TO 4 IN-LB ± .5 IN-LB.
2. TORQUE TO 3 IN-LB ± .5 IN-LB.
3. AFTER INSERTING CONNECTOR ON SEQ. NO. 22 INTO OPENING IN SEQ. NO. 20, FOLD TOP PART OF SEQ. NO. 20 DOWN OVER SEQ. NO. 22. WEBS BREAKING ON SEQ. NO. 20 IS ACCEPTABLE.
4. ENCLOSURE TO BE ORIENTED WITH SMALLER GUIDE GROOVE AT TOP.
6. INSERT SEQ.NO. 29 THROUGH THE CONCENTRIC HOLES ON SEQ.NO. 22 AND GROUND CLIP AND SCREW SEQ.NO. 29 IN PLACE. TORQUE TO 3 IN-LB ± .5 IN-LB.
7. TO MEET PATIENT SAFETY REQUIREMENTS, VERIFY PROPER INSULATOR INSTALLATION. ENSURE THAT LONG NOTCH END IS TOWARD REAR OF MODULE.

FO-32B. Top Assembly 7310

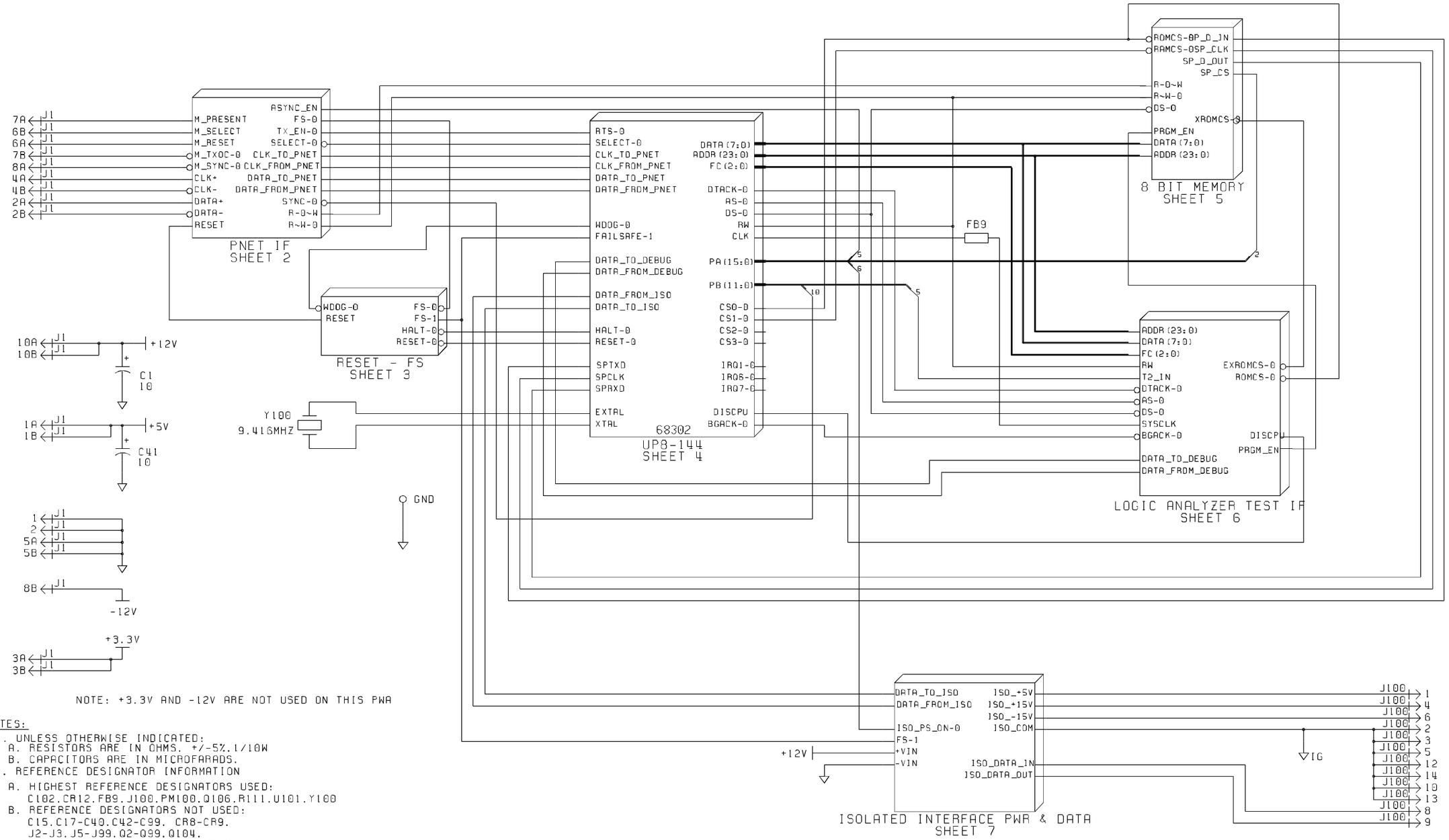


NOTES.

3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

⚠6 PROGRAM DEVICE PRIOR TO INSTALLATION.

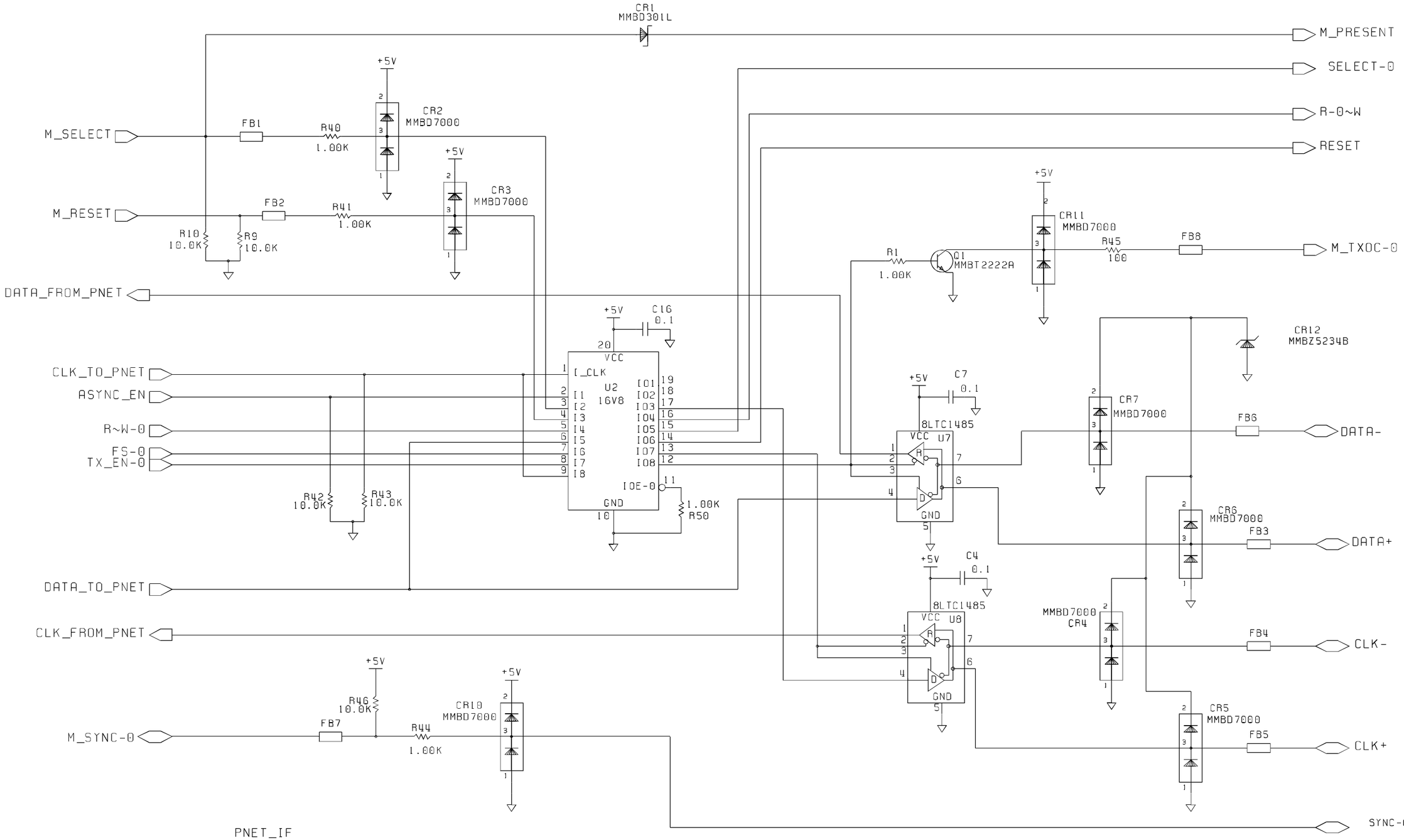
FO-32C. SpO2 Digital PWA 315-440



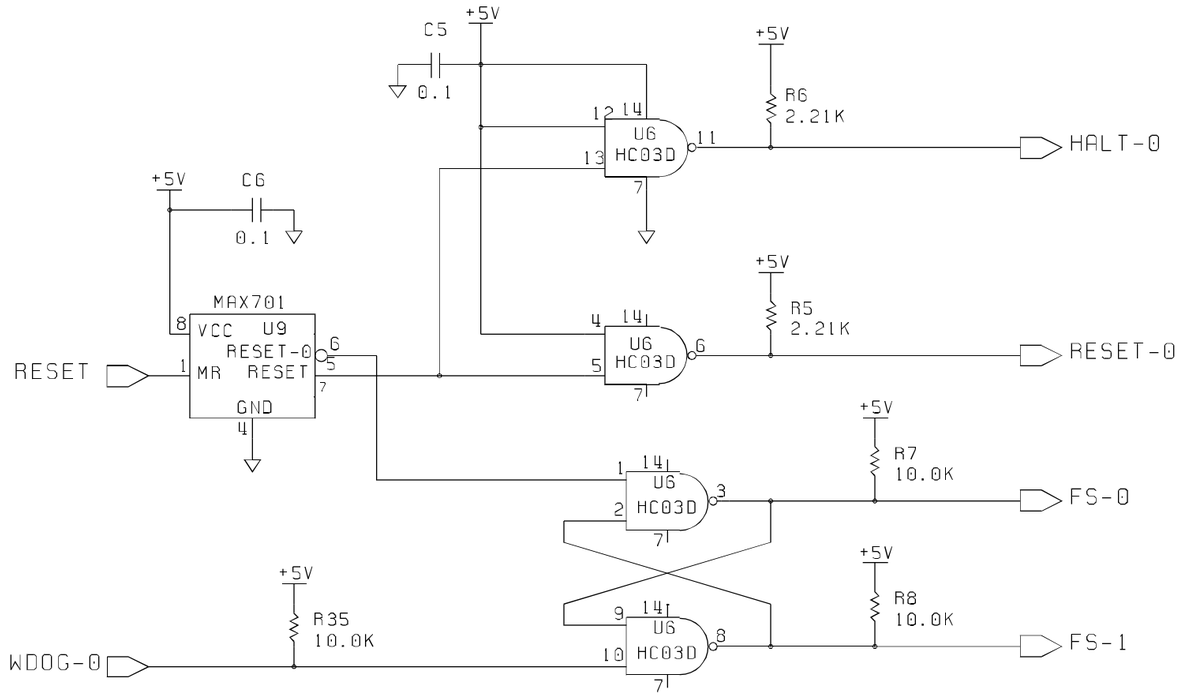
NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS. +/-5%.1/10W
   B. CAPACITORS ARE IN MICROFARADS.
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C102.CR12.FB9.J100.PM100.Q106.R111.U101.Y100
   B. REFERENCE DESIGNATORS NOT USED:
      C15.C17-C40.C42-C99. CR8-CR9.
      J2-J3.J5-J99.Q2-Q99.Q104.
      R36-39.R47-49.R51-99.R110.U5.U12-99.

SC315-440 A
SpO2 Digital PWA Schematic (1 of 7)

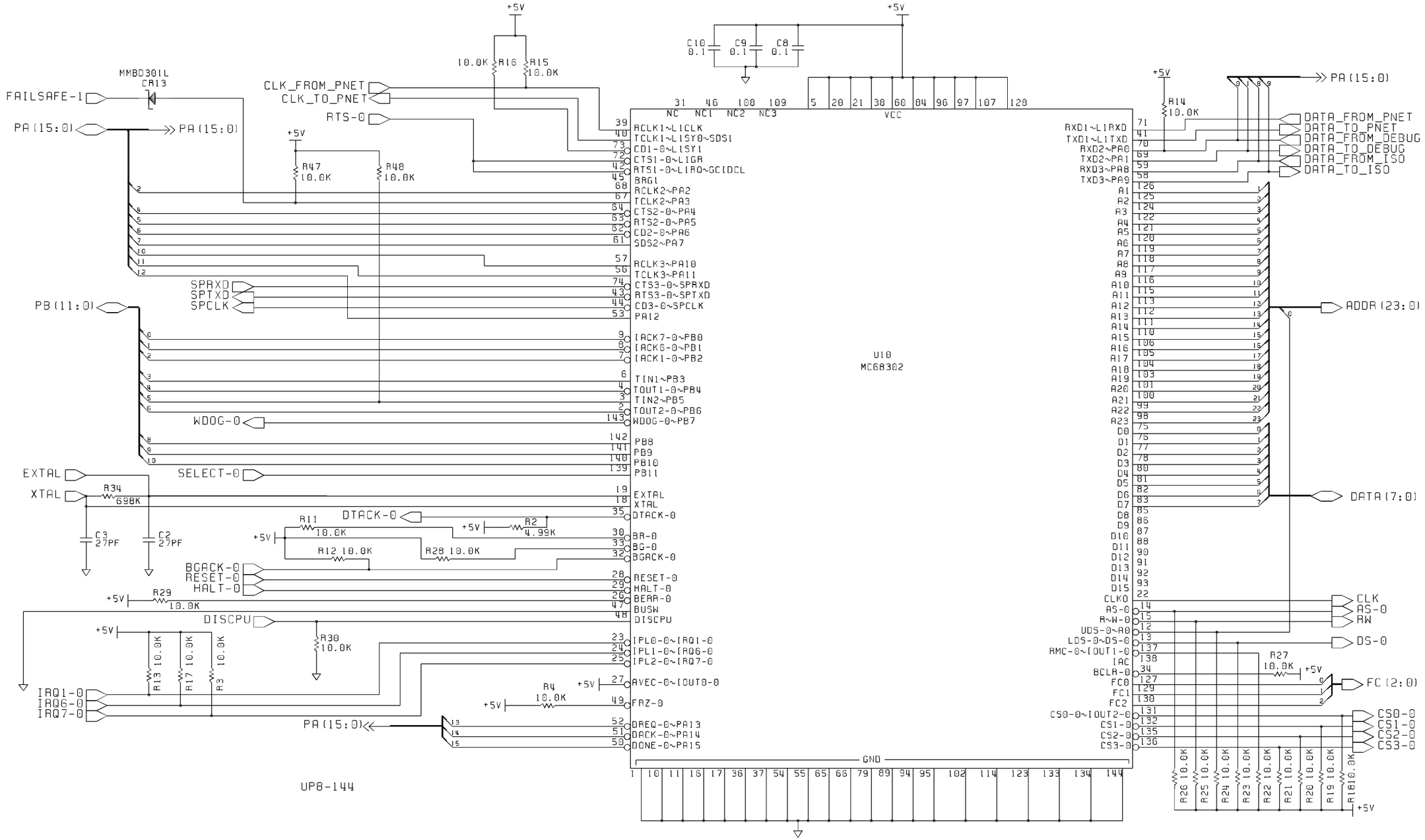


SC315-440 A
SpO2 Digital PWA Schematic (2 of 7)

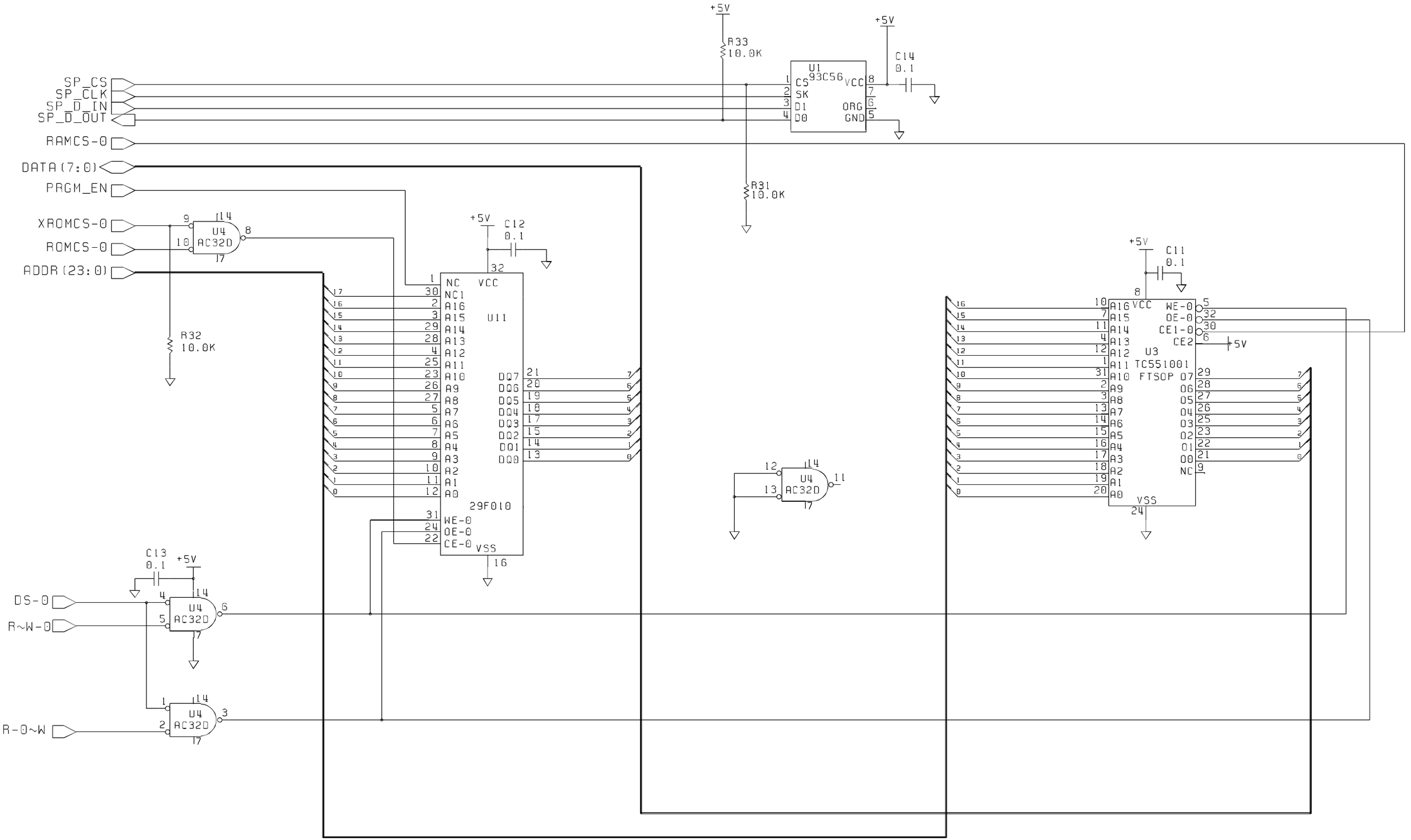


RESET - FS

SC315-440 A
SpO2 Digital PWA Schematic (3 of 7)

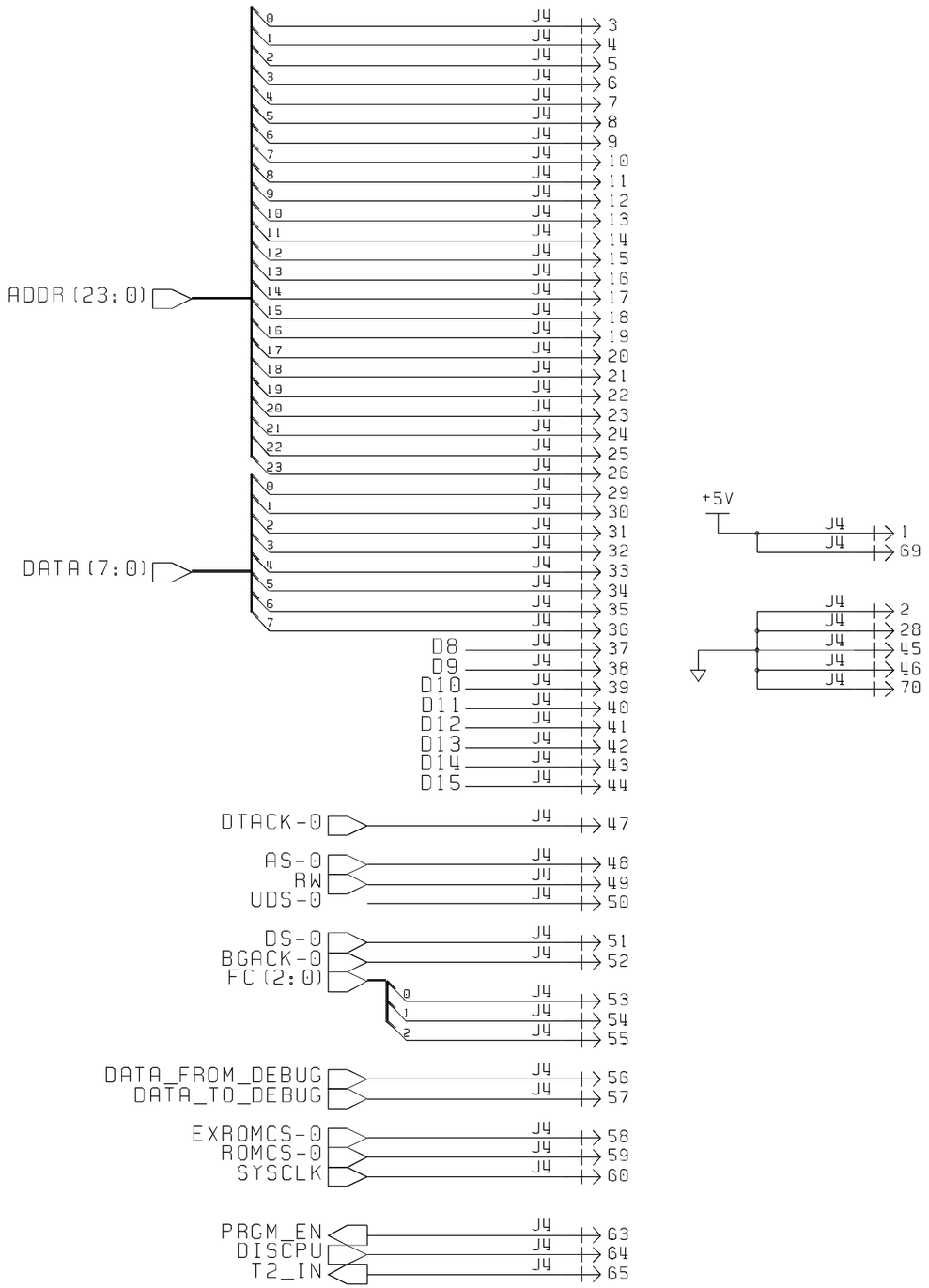


SC315-440 A
SpO2 Digital PWA Schematic (4 of 7)



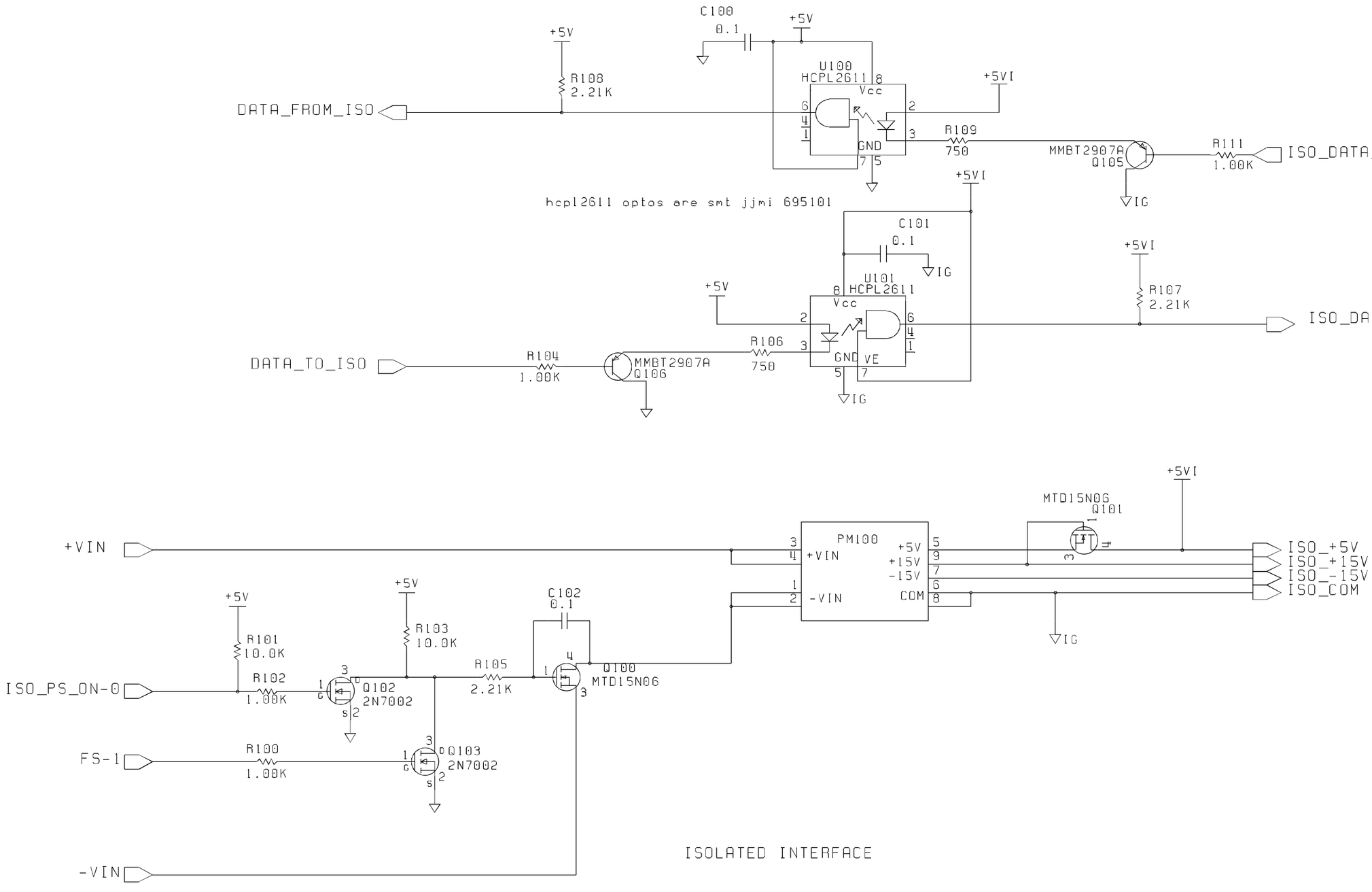
8 BIT MEMORY_2

SC315-440 A
SpO2 Digital PWA Schematic (5 of 7)



LOGIC ANALYZER TEST IF_4

SC315-440 A
SpO2 Digital PWA Schematic (6 of 7)



SC315-440 A
SpO2 Digital PWA Schematic (7 of 7)